U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,988,190	01-2006	Park, Sung-Bae	712/241
*	B	US-6,304,962	10-2001	Nair, Ravindra K.	712/240
*	C	US-5,381,533	01-1995	Peleg et al.	712/215
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Ramirez et al., "Fetching Instruction Streams", Proceedings of the 35th Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-35, Nov. 18-22, 2002, pp. 371-382. ✓
	V	Rotenberg et al., "A Trace Cache Microarchitecture and Evaluation", IEEE Transactions on Computers, vol. 48, iss. 2, Feb. 1999, pp. 111-120 ✓
	W	Hank et al., "Superblock Formation Using Static Program Analysis", Proceedings of the 26th International Symposium on Microarchitecture, Dec. 1-3, 1993, pp. 247-255. ✓
	X	Patel et al., "Critical Issues Regarding the Trace Cache Fetch Mechanism", Technical Report, CSE TR-335-97, University of Michigan, May 1997, pp. 1-33. ✓

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lee et al., "On Augmenting Trace Cache for High-Bandwidth Value Prediction", IEEE Transactions on Computers, vol. 51, iss. 9, Sept. 2002, pp. 1074-1088. ✓
	V	Rotenberg et al., "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching", Proceedings of the 29th Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-29, Dec. 2-4, 1996, pp. 24-34. ✓
	W	Jacobson et al., "Path-Based Next Trace Prediction", Proceedings of the 30th Annual IEEE/ACM International Symposium on Microarchitecture, Dec. 1-3, 1997, pp. 14-23. ✓
	X	Rakvic et al., "Completion Time Multiple Branch Prediction for Enhancing Trace Cache Performance", Proceedings of the 27th International Symposium on Computer Architecture, 2000, pp. 47-58. ✓

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

		Application/Control No.	Applicant(s)/Patent Under Reexamination
Notice of References Cited		10/608,316	WANG ET AL.
		Examiner	Art Unit	
		William M. Treat	2181	Page 3 of 3

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Nair et al., "Exploiting Instruction Level Parallelism in Processors by Caching Scheduled Groups", Proceedings of the 24th Annual International Symposium on Computer Architecture, June 2-4, 1997, pp. 13-25.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.